Principles of Micro- and Nanofabrication for Electronic and Photonic Devices

Film Deposition Part II: Si Oxidation

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CMOS Transistors

1. Grow field oxide
   - p-type substrate

2. Etch oxide for pMOSFET
   - p-type substrate

3. Diffuse n-well
   - p-type substrate

4. Etch oxide for nMOSFET
   - p-type substrate

5. Grow gate oxide
   - p-type substrate

6. Deposit polysilicon
   - p-type substrate

7. Etch polysilicon and oxide
   - p-type substrate

8. Implant sources and drains
   - p-type substrate

9. Grow nitride
   - p-type substrate

10. Etch nitride
    - p-type substrate

11. Deposit metal
    - p-type substrate

12. Etch metal
    - p-type substrate
Properties of SiO$_2$

- Very stable
  - for Ge, GeO$_2$ is soluble in water, and decompose at 450 °C
  - for GaAs, GaO$_x$ and AsO$_x$ have many defects

- Easily etched
  - wet etch (HF solution) or dry etch (F based plasma)

- Good diffusion barrier (low dopant diffusivity $D_{ox} << D_{Si}$)

- High quality insulator
  - band gap ~ 8 eV, resistivity $> 10^{16}$ Ω*cm

- High dielectric strength ($> 500$ V/μm)

- Low interface state / defect density ($< 10^{10}$ cm$^{-2}$)
# Properties of SiO₂

## Table 9.3 Properties of Thermal Silicon Dioxide

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC resistivity (Ω · cm), 25°C</td>
<td>10¹⁴–10¹⁶</td>
<td>Melting point (°C)</td>
<td>~1700</td>
</tr>
<tr>
<td>Density (g/cm³)</td>
<td>2.27</td>
<td>Molecular weight</td>
<td>60.08</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>3.8–3.9</td>
<td>Molecules/cm³</td>
<td>2.3 × 10²²</td>
</tr>
<tr>
<td>Dielectric strength (V/cm)</td>
<td>5–10 × 10⁶</td>
<td>Refractive index</td>
<td>1.46</td>
</tr>
<tr>
<td>Energy gap (eV)</td>
<td>~8</td>
<td>Specific heat (J/g · °C)</td>
<td>1.0</td>
</tr>
<tr>
<td>Etch rate in buffered HF (nm/min)</td>
<td>100</td>
<td>Stress in film on Si (N/m²)</td>
<td>2–4 × 10⁸</td>
</tr>
<tr>
<td>Infrared absorption peak (µm)</td>
<td>9.3</td>
<td>Compression</td>
<td></td>
</tr>
<tr>
<td>Linear expansion coefficient (°C⁻¹)</td>
<td>5.0 × 10⁻⁷</td>
<td>Thermal conductivity (W/cm · °C)</td>
<td>0.014</td>
</tr>
</tbody>
</table>

*Source: After Wolf and Tauber (1986).*

*Buffered HF: 28 ml HF, 170 ml H₂O₂, 113 g NH₄F.*

## Table 7.2 Diffusivities of Elements in SiO₂

<table>
<thead>
<tr>
<th>Element</th>
<th>D at 1100°C (cm²/s)</th>
<th>D at 1200°C (cm²/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>3 × 10⁻¹⁷ to 2 × 10⁻¹⁴</td>
<td>2 × 10⁻¹⁶ to 5 × 10⁻¹⁴</td>
</tr>
<tr>
<td>Ga</td>
<td>5.3 × 10⁻¹¹</td>
<td>5 × 10⁻⁸</td>
</tr>
<tr>
<td>P</td>
<td>2.9 × 10⁻¹⁶ to 2 × 10⁻¹³</td>
<td>2 × 10⁻¹⁵ to 7.6 × 10⁻¹³</td>
</tr>
<tr>
<td>Sb</td>
<td>9.9 × 10⁻¹⁷</td>
<td>1.5 × 10⁻¹⁴</td>
</tr>
<tr>
<td>Ar</td>
<td>1.2 × 10⁻¹⁶ to 3.5 × 10⁻¹⁵</td>
<td>2 × 10⁻¹⁵ to 2.4 × 10⁻¹⁴</td>
</tr>
</tbody>
</table>
Si forms native oxide in the air (1~2 nm, a few hours)

Q: amorphous or crystalline SiO$_2$?
Thermal Oxide Growth

**Dry Oxidation**

$$\text{Si (s)} + \text{O}_2 (g) = \text{SiO}_2 (s)$$

**Wet Oxidation**

$$\text{Si (s)} + \text{H}_2\text{O (g)} = \text{SiO}_2 (s) + \text{H}_2 (g)$$

Video
The Deal-Grove (D-G) Model

- **Stagnant layer**
  - $C_G \rightarrow C_s$

- **SiO$_2$**
  - $C_s \neq C_o$
  - $F_2$: diffusion flux through SiO$_2$

- **Si**
  - $C_i$

**Fluxes**

- $F_1$: gas transport flux
- $F_2$: diffusion flux through SiO$_2$
- $F_3$: reaction flux at interface

**Note**
- $F$: oxygen flux – the number of oxygen molecules that crosses a plane per unit area per second
The Deal-Grove (D-G) Model

\[ X_{ox} = \frac{A}{2} \left\{ \sqrt{1 + \left( \frac{t + \tau}{A^2 / 4B} \right)} - 1 \right\} \]

- \( A \): related to reaction
- \( B \): related to diffusion
- \( \tau \): initial native oxide

**Linear Growth Regime** (reaction limited)

\[ X = \frac{B}{A} t \]

**Diffusion-Limited Regime**

\[ X = \sqrt{B t} \]
Thermal Oxidation

- **Process Parameters**
  - Time
  - Temperature
  - Gas type (O$_2$, H$_2$O, ...)
  - Gas pressure
  - Crystal orientation
  - Dopant (B, P, As, ...)

- **Control Parameters**
  - Oxide thickness
  - Film quality (defects, dielectric strength, ...)

\[
X_{ox} = \frac{A}{2} \left\{ \sqrt{1 + \left( \frac{t + \tau}{A^2} \right)} - 1 \right\}
\]

Linear Growth Regime

\[
X = \frac{B}{A} t
\]

Diffusion-Limited Regime

\[
X = \sqrt{Bt}
\]
Dry vs. Wet Oxidation

Wet oxidation is 10~100 times faster than dry oxidation because $\text{H}_2\text{O}$ has higher solubility/diffusivity in $\text{SiO}_2$. 

Video
Crystal Orientation

Si (111) has smaller $A$, but same $B$ with Si (100)

higher growth rate at initial stage

why ??
Crystal Orientation

Si (100)  Si (111)

similar rates at long time oxidation (diffusion limited)
Thermal Oxidation - Simulation

Oxide Growth Calculator

**Time Given Desired Thickness**

<table>
<thead>
<tr>
<th>Initial Thickness:</th>
<th>25</th>
<th>Å</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Thickness:</td>
<td>10000</td>
<td>Å</td>
</tr>
<tr>
<td>Temperature:</td>
<td>1100 °C (700 to 1200)</td>
<td></td>
</tr>
<tr>
<td>Crystal Orientation:</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Environment:</td>
<td>Wet</td>
<td></td>
</tr>
<tr>
<td>Oxidation Time:</td>
<td>2:14:18 hrs:mins:secs</td>
<td></td>
</tr>
</tbody>
</table>

**Thickness Given Time**

<table>
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<th>25 Å</th>
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<td>100</td>
</tr>
<tr>
<td>Environment:</td>
<td>Wet</td>
</tr>
<tr>
<td>Oxidation Time:</td>
<td>hrs: 1 mins: 0</td>
</tr>
<tr>
<td>Thickness:</td>
<td>Å</td>
</tr>
</tbody>
</table>

[https://cleanroom.byu.edu/processes#Microfab_OxideGrowth](https://cleanroom.byu.edu/processes#Microfab_OxideGrowth)
SiO₂ Film Thickness Measurement

color difference
SiO$_2$ Film Thickness Measurement

Spectroscopic Ellipsometer
SiO$_2$ in CMOS

gate oxide for transistors

\[ I_{D,\text{Sat}} = \frac{W}{L} \mu C \left( V_G - V_{th} \right)^2 \]
SiO$_2$ in CMOS

Local Oxidation of Si (LOCOS)

For isolation

transistor region
SiO$_2$ in CMOS

Q: why?

other methods to deposit SiO$_2$

temperature
SiO$_2$ in CMOS

\[ C = \frac{\kappa \varepsilon_0 A}{t} \]

- low $\kappa$ dielectric for insulating reduce RC delay
- high $\kappa$ dielectric for gate oxide

\[ I_{D,Sat} = \frac{W}{L} \mu C \left( V_G - V_{th} \right)^2 \]
Oxide for High $\kappa$ Dielectric

$$I_{D,Sat} = \frac{W}{L} \mu C \left( V_G - V_{th} \right)^2$$

$$C = \frac{\kappa \varepsilon_0 A}{t}$$

thickness $t$ is already $\sim$ nm
high $\kappa$ -> large $C$ -> large $I_D$
Porous SiO$_2$ for Low $\kappa$ Dielectric

SiO$_2$

$\kappa = 3.9$

air

$\kappa = 1.0$
SiO$_2$ in Biointegrated Devices

Thermal oxide is an ideal moisture barrier useful for implantable devices

At room temperature, it will take $> 100$ years to dissolve 1 $\mu$m thermal SiO$_2$ in water