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Plasmon-Induced Heterointerface Thinning for Schottky Barrier Modification of Core/Shell SiC/SiO_2 Nanowires

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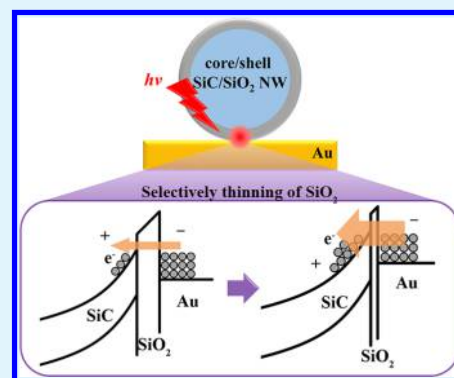
Supporting Information

ABSTRACT: In this work, plasmon-induced heterointerface thinning for Schottky barrier modification of core/shell SiC/SiO_2 nanowires is conducted by femtosecond (fs) laser irradiation. The incident energy of polarized fs laser (50 fs, 800 nm) is confined in the SiO_2 shell of the nanowire due to strong plasmonic localization in the region of the electrode−nanowire junction. With intense nonlinear absorption in SiO_2, the thickness of the SiO_2 layer can be thinned in a controllable way. The tuning of the SiO_2 barrier layer allows the promotion of electron transportation at the electrode−nanowire interface. The switching voltage of the rectifying junction made by the SiC/SiO_2 nanowire can be significantly tuned from 15.7 to 1 V. When selectively thinning at source and drain electrodes and leaving the SiO_2 barrier layer at the gate electrode intact, a metal/oxide/semiconductor (MOS) device is fabricated with low leakage current. This optically controlled interfacial engineering technology should be applicable for MOS components and other heterogeneous integration structures.



KEYWORDS: *interface modification, core/shell, SiC, plasmonic effect, field-effect transistor, femtosecond laser*

INTRODUCTION

The metal/semiconductor heterointerface is of great interest for nanoelectronic devices because of their band alignment, which affects the interfacial barriers and overall performance of devices.[1−5] For example, Schottky- or Ohmic-like behavior has been observed at size-selected metal/semiconductor interfaces due to geometric effects influencing the contact depletion region, leading to enhanced tunneling at the contact.[6−8] Even though the size of the contact area between the metal and semiconductor is kept constant, the contact resistance could also be affected by disorders or noncrystalline interfacial defects, which may elevate the interfacial resistance by two or three orders of magnitude.[9] Therefore, to tune the electrical properties and improve the performance of devices, it is of vital importance to modify metal/semiconductor interfaces in a controllable manner.

To date, there are already several high-tech doping methods, such as spin-coating[10] and acid processing,[11] but most of them are environmentally unfriendly and costly. Recently, surface plasmon has been widely adopted for heterointerface modification and band engineering.[12−14] It has been reported that the hot electrons generated by the plasmons are injected across the Au/ZnO interface into the conduction band of the semiconductor, which promotes the separation of photogenerated electrons and holes.[13] Similar devices could also be applied in plasmonic solar water splitters, where the hot electrons resulting from the excitation of surface plasmons enhance the oxidation and reduction steps.[14] However, a plasmon excitation source with high power, such as continuous wave laser, would induce huge heat-affected zones because of the thermal effect, and even material and substrate damages.[15] Compared with other light sources, femtosecond (fs) laser with an ultrashort pulse width and extremely high peak intensity allows the strong electric field effect to be confined in a small space, which can be used for precise material processing.[16,17] Meanwhile, a focused fs laser beam could easily trigger strong surface plasmon enhancement at different metal−semiconductor interfaces, which can realize low-power modification.[18]

Recently, considerable effort has been devoted to modifying core/shell nanostructure systems for energy storage and photoelectronic applications, due to the large surface area and the continuous electron transport among metal/semiconductor interfaces. For example, Hou et al.[19] report nitrogen-doped carbon/CuCo/$CuCoO_x$ architectures, as both electrodes for water splitting exhibit a current density of 10 mA cm^{-2} at a cell voltage of 1.53 V with excellent stability. SiC nanowires (NWs), with their wide band gap, have

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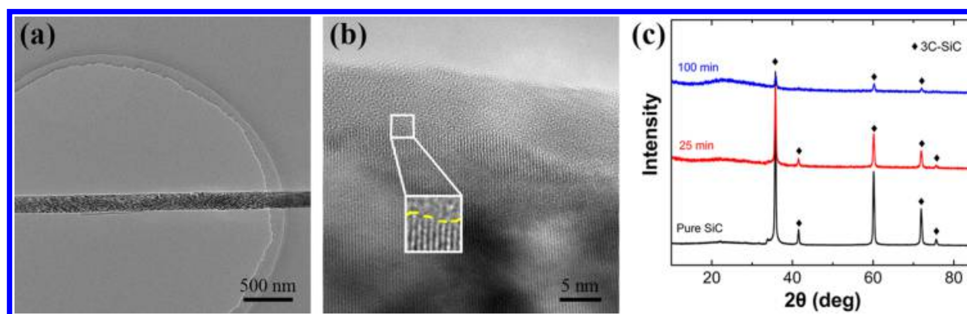

Figure 1. (a) TEM image of a single core/shell SiC/SiO_2 NW annealed in O_2 atmosphere at 900 °C for 25 min. (b) High-resolution TEM image of the NW in (a). Inset is a magnified image of the SiO_2/SiC interface. (c) XRD spectra of SiC NWs annealed for 0 min (pure SiC), 25, and 100 min.

applications in nanoelectronic devices.[20,21] On the other hand, SiC NWs accompanied with SiO_x will allow the formation of a complex interfacial status and electronic band structures, which show great potential in metal/oxide/semiconductor (MOS)-based devices.[22]

In this study, a method for plasmon-induced heterointerface thinning is developed for Schottky barrier modification in SiC NW devices. Core/shell SiC/SiO_2 NWs with different thicknesses of the SiO_2 shell are employed to fabricate three-terminal structured devices on Au electrodes. A focused fs laser beam illuminates the source and drain of the device, thinning the oxide layer due to localized plasmon enhancement and nonlinear absorption at the electrode−NW contact. To understand the changes of transport mechanisms at the modified MOS interfaces, the obtained current−voltage (*I*−*V*) curves and cross sections of MOS structures are analyzed in detail. By plasmonic interfacial thinning at the $Au/SiO_2/SiC$ interface, single NW-based field-effect transistors (FETs) with a controllable leakage current are studied.

EXPERIMENTAL SECTION

Materials and Device Fabrication. SiC NWs were purchased from XFNANO Materials (Nanjing, China) with pure-phase 3C-SiC without oxides on the surface. The SiC NWs were then annealed in a tubular furnace in O_2 atmosphere with a pressure of 0.02 MPa at 900 °C. In this study, holding durations of 25, 50, 100, and 200 min were used to obtain different oxide layers on SiC NWs. After oxidation, NWs were dispersed in high-purity ethanol (99.5%). The solution was drop cast on prefabricated Au interdigital electrodes, which were sputtered on an undoped silicon chip (with a 300 nm thick SiO_2 layer) using conventional photolithography and lift-off process with a finger spacing of 3 μm. After the solution dried in the air, the electrodes were then placed on a heating plate for further removal of organics on NWs at 90 °C for 30 min.

Fs laser with a wavelength of 800 nm and pulse width of 50 fs was generated by a Ti:Sapphire system at 1 kHz, and was employed for localized irradiation. The laser beam was pointed at the source and drain of the device by an objective lens with a numerical aperture of 0.5. The laser irradiation time was controlled by a program-controlled shutter. The incident polarization on the NW was then controlled by a linear polarizer to adjust the angle with the NW. The laser fluence irradiated on the samples was tuned by a neutral density filter with different absorbances.

Materials Characterization. The morphologies of SiC NWs and core/shell SiC/SiO_2 NWs were characterized by scanning electron microscopy (SEM, Zeiss Supra 55). NWs' crystallinity was studied by X-ray diffraction (XRD, Bruker D8), and the surface chemical states were measured by X-ray photoelectron spectroscopy (XPS, Thermo Fisher Scientific ESCALAB 250Xi). To characterize the cross section of the Au/SiC interface, a focused ion beam (FIB, Tescan LYRA3) was used to prepare TEM lamella. Transmission electron microscopy (TEM, JEM-2100F) and energy-dispersive X-ray spectroscopy (EDX) were conducted for the phase and crystal structure analyses.

Electrical Measurements. *I*−*V* characteristics of as-fabricated devices were tested by a precise source-meter (Agilent B2911A). The gate voltage was supplied by a direct current voltage source (DPS-305BM), and was operated manually. Typical linear wave voltage sweeps with various amplitudes were programmed at a sweeping rate of 0.2 V s^{-1}. Three profiles were introduced in the testing source programs: (a) −5 → 5 V, (b) −15 → 15 V, and (c) −20 → 20 V.

Simulations. The electric field distribution under fs laser irradiation was simulated by a commercial finite element method software (COMSOL Multiphysics 5.2a) with an RF module. Details of the simulation model, including geometry size and light source parameters, are provided in Figure S1 in Supporting Information. Linearly polarized plane wave was used to simulate fs laser pulses at a wavelength of 800 nm.

RESULTS AND DISCUSSION

Figure 1a,b shows the TEM images of a single core/shell SiC/SiO_2 NW. A clear heterogeneous boundary between the amorphous shell and the SiC core is observed. The highly oriented SiC core still retains a 3C phase, which is consistent with the pure SiC NW before annealing (Figure 1c). After thermal annealing for 25, 100, and 200 min, the average thicknesses of oxide layers are 7.8, 35.7, and 45 nm, respectively (Figure S2 in Supporting Information). The diameters of core/shell SiC/SiO_2 NWs range from 100 to 200 nm, and only Si and O elements exist in the amorphous layer (Figures S3 and S4 in Supporting Information).

To verify the stoichiometric state of this oxidized amorphous layer, high-resolution XPS was conducted, and the results including Gaussian deconvolution peak fittings of Si 2p and O 1s are shown in Figure 2. Increasing the annealing time can weaken the peak centered at 100.8 eV in Si 2p and boost the appearance of a new peak at 103.7 eV, which represent SiC and SiO_2, respectively.[23] The peak at 534 eV is attributed to the O 1s spectrum, representing SiO_2.[24] The weak peak at 532 eV (O 1s) is expected to be due to the surface absorption of oxygen in the air. The above results confirm the core/shell nanowire structure. The SiO_2 shell could be a stable insulation barrier to block electron conduction in the nanoelectronics.[25]

Figure 3a,b shows the schematic diagram of the device fabrication process and the image of the assembled device, respectively. To understand the influence of the oxide layer on the electrical properties of the heterointerface, the source−drain current (I_{sd}) is first measured under 0 V gate voltage (V_g) (Figure 3c). The compliance current is 1 μA. The *I*−*V* curve of pure SiC NW demonstrates a nonlinear relationship, indicating a couple of back-to-back Schottky barriers in the symmetrical structure. As the applied voltage increases, the reverse barrier

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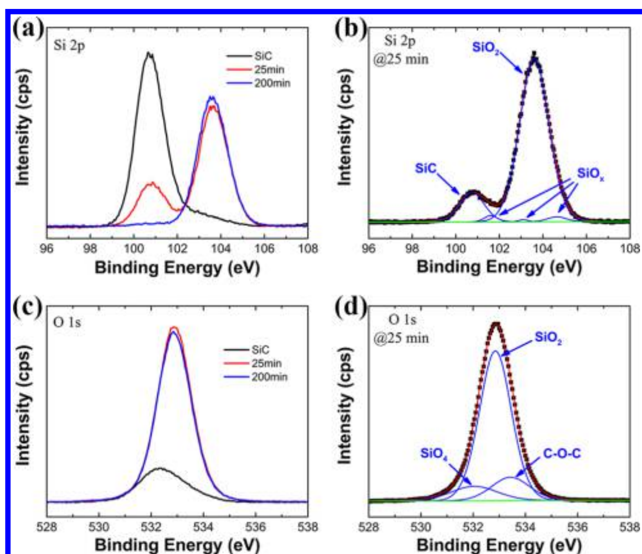

Figure 2. XPS spectra of oxidized SiC NWs under different thermal conditions: (a) Si 2p spectra for different annealing times; (b) Si 2p spectra for 25 min; (c) O 1s spectra for different annealing times; (d) O 1s spectra for 25 min.

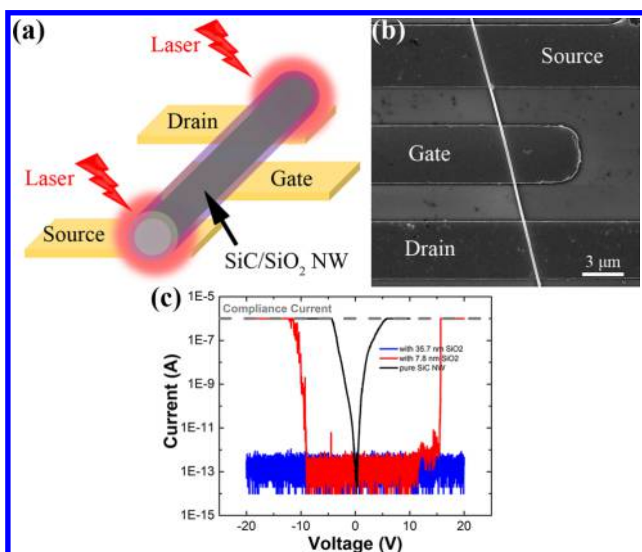

Figure 3. (a) Schematics of a core/shell SiC/SiO_2 NW-based three-terminal device. (b) SEM image of an as-fabricated NW device. (c) $I-V$ characteristics of core/shell SiC/SiO_2 NWs with average oxide thicknesses of 0, 7.8, and 35.7 nm. The source−drain voltage is −20 → 20 V and the gate voltage is 0 V.

always decides the measured current. The observed high current appears at 5.7/−4.3 V, which indicates a reverse breakdown. For the unit with the 7.8 nm SiO_2 layer, I_{sd} exhibits a low level at the beginning, and then an abrupt increase appears at +15.7 V under forward biasing. The typical tunneling characteristic of I_{sd} is mainly due to the inserted SiO_2 layer. As the thickness of the inserted insulator increases, it becomes more difficult for the carriers to tunnel through the heterojunction, and the tunneling barrier is the dominant factor of the total barrier height, which decreases the current density in the end.[26] Recently, for the high current arising in the back-to-back Schottky barriers, a model is proposed by Bartolomeo et al.[27] that the image force barrier lowering affects the current mainly when the forcing electrode is on the reverse-biased junction. However, the image force usually causes less than 0.1 eV barrier lowering, which can be neglected due to the high oxide barrier.[28] This was further verified by measuring the NW with 35.7 nm SiO_2. When the bias voltage ranges from −20 to 20 V, I_{sd} remains around 100 fA. These results indicate that SiO_2 shells do affect the carrier transportation across the heterointerface. The existence of a thin SiO_2 layer can be considered as an interface barrier, which promotes a large switch ratio in such devices (e.g., 7.8 nm). By contrast, a thick SiO_2 layer works as an absolute insulator that prohibits carrier transportation across the Au/SiC contact (e.g., 35.7 nm).

Fs laser irradiation on the metal/semiconductor heterojunction is able to modify the contact, which in turn can change electrical conduction.[12] Figure 4a shows the $I-V$ curves

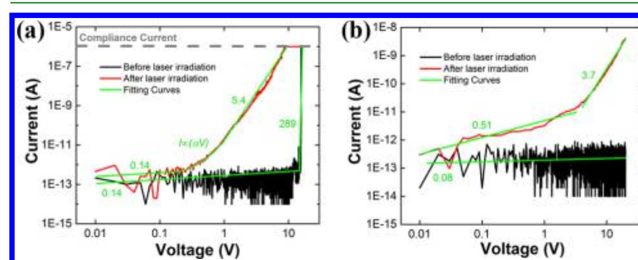

Figure 4. $I-V$ curves of the as-received SiC NW structure before and after fs laser irradiation at a fluence of 72.9 mJ cm^{-2}: (a) the 7.8 nm SiO_2 shell for 10 s and (b) the 35.7 nm SiO_2 shell for 120 s. The gate voltage is 0 V.

of a SiC NW with an average oxide thickness of 7.8 nm. Before fs laser irradiation, the $I-V$ curve shows two stages as the applied voltage increases. After 10 s of fs laser irradiation at 72.9 mJ cm^{-2}, the $I-V$ curve changes to three stages: (i) When the bias voltage is <0.26 V, the $I-V$ curve shows a slight linear increase with a slope of <1. (ii) As the bias voltage increases from 0.26 to 1 V, the I_{sd} increases exponentially. (iii) When the bias voltage is >1 V, the $I-V$ curve shows a linear fit with a large slope of 5.4. Comparison of the two curves shows that the insulator barrier at the $Au/SiO_2/SiC$ interface can be reduced by an fs laser. If the SiO_2 shell is thick (35.7 nm), extending the irradiation time to 120 s can only increase the slope of the $I-V$ curve from 0.08 to 3.7 (Figure 4b). The I_{sd} could only reach ∼4 nA without reverse breakdown when the bias voltage is 20 V. It is expected that the extent of insulator barrier reduction by the fs laser is determined by the original thickness of the SiO_2 shell.

To investigate the effect of the fs laser on the SiO_2 shell, a TEM cross section of the core−shell nanowire and Au electrode interface is prepared by the FIB lift-out method (Figure 5a). The sample is prepared with SiC NWs annealed for 100 min, and the laser irradiation time is 120 s. The SiO_2 shell evenly covers the nanowire before irradiation. After fs laser irradiation, the thickness of the SiO_2 shell at the bottom (∼14.2 nm) is much thinner than that at the top (∼37.8 nm) as shown in Figure 5b, which is also confirmed by EDX mapping (Figure S5 and S6 in Supporting Information). A closer inspection at the interface between the Au electrode and the SiC NW reveals that most regions show a bonded interface between the nanowire and the electrode, except a few regions without contact (red dashed circle) (Figure 5c). The high-resolution TEM image in Figure 5d shows a clear boundary without obvious crystal defects at the SiC/SiO_2 interface.

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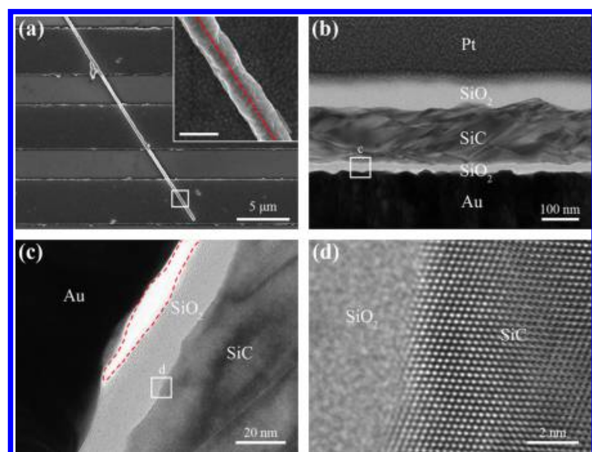

Figure 5. (a) SEM image of SiC/SiO_2 NW on Au electrodes (SiO_2 layer with an average thickness of 35.7 nm) after fs laser irradiation at a fluence of 72.9 mJ cm^{-2} for 120 s. Inset is the zoom-in image. Inset scale bar is 400 nm. (b) TEM image of a cross section of the Au/ SiC structure, from the slice marked with a red dashed line in the inset in (a). (c) The zoom-in image of the rectangle in (b). (d) The zoom-in high-resolution TEM image of the rectangle in (c).

These microstructure results clearly indicate a selective thinning effect by fs laser irradiation. In the meantime, no damage is generated at the Au electrode and the SiC core.

Figure 6 shows the simulated electrical field distribution in the NW−electrode structure upon fs laser irradiation. When

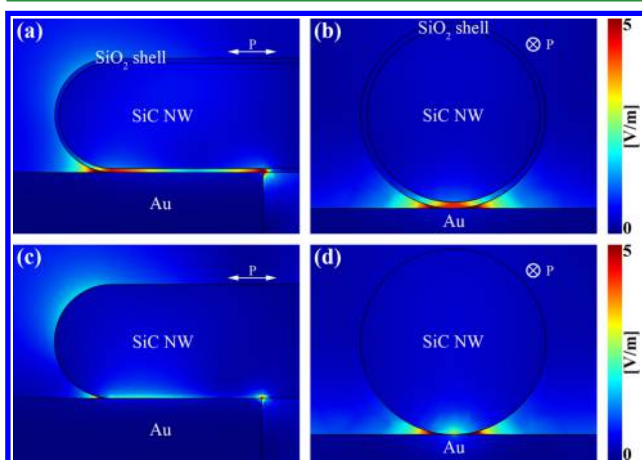

Figure 6. Simulations of electric field distribution around the Au/ SiO_2/SiC heterointerface under fs laser irradiation at a wavelength of 800 nm. The color scale indicates the magnitude of the generated electric field. Laser polarization is parallel to the long axis of the SiC NW. (a, b) With a 7 nm SiO_2 shell; (c, d) without the SiO_2 shell.

the polarization direction is parallel to the long axis of the NW (Figure 6a,b), the electric field is mainly enhanced within the SiO_2 shell, which is consistent with the thinning region described above. This localized field enhancement results in the formation of a "hotspot", which facilitates energy absorption.[29] It is known that the efficiency of "hotspot" heating is influenced by the polarization and wavelength of the incident laser. The enhancement could be maximized when they match the surface plasmon resonance condition of the structure.[29,30] Results show that under 800 nm wavelength laser excitation, the surface plasmon resonance can be effectively excited (Figure S7 in Supporting Information). The efficient thinning could be realized by the plasmonic absorption of the high peak energy of fs laser pulses.[31,32] If the polarization direction is perpendicular to the long axis of the NW, the electric field enhancement is not mainly focused on the SiO_2 layer at the nanowire−electrode interface, the intensity of which becomes smaller with the same incident energy (Figure S8 in Supporting Information). Except for the polarization and wavelength, the core/shell structure also contributes to the distribution of electric field. Figure 6c,d shows that without the SiO_2 layer, the enhancement is still at the Au and SiC NW contact and the incident laser energy is mainly absorbed by SiC. Due to the difference of the refractive index between SiO_2 and SiC, the Au/SiO_2/SiC sandwich structure effectively confines the laser energy within the SiO_2 shell. The intensity of the enhanced electric field is highly affected by the thickness of the SiO_2 layer, which becomes larger with the SiO_2 thinning (Figure S9 in Supporting Information). In any cases, the fs laser irradiation can thin the SiO_2 layer without affecting the Au electrode and SiC nanowire.

Based on the theory of semiconductor band, the energy band diagram of the back-to-back Au/SiO_2/SiC heterointerface is shown in Figure 7a. The original pure SiC NW shows an

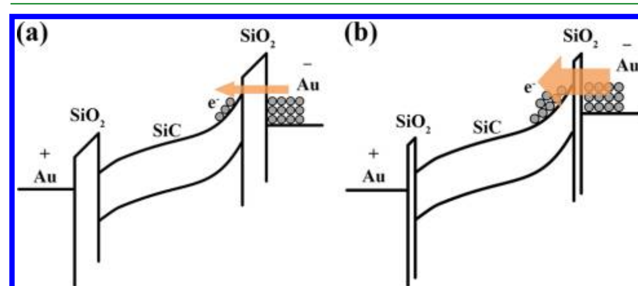

Figure 7. Energy band diagrams of the back-to-back Au/SiO_2/SiC interface under an applied bias voltage. (a) With the initial SiO_2 layer. (b) With the laser-thinned SiO_2 layer.

n-type doping property (Figure S10 in Support Information). Due to the existence of a SiO_2 layer, the barrier is different from a typical Schottky contact. A superhigh barrier height is provided, which prohibits electron transportation by thermionic emission. Then, the electrons can move across the interface barrier only by tunneling effect until a threshold voltage is reached, which will cause electrical breakdown. The approximate general equation of the tunneling current density is given by[33]

$$J = \frac{4\pi q m_0}{h^3} \int_{E_c}^{E_{max}} T(E) kT \ln\left(1 + \exp\left(-\frac{E - E_F}{kT}\right)\right) dE \quad (1)$$

where $E_{max} = q\Phi$ and m_0 is the free electron mass. Although eq 1 only describes a single MOS interface, the current density under reverse bias voltage can represent the electrical property of the back-to-back structure. According to this model, the direct tunneling current through the SiO_2 becomes significant when its thickness is below 5 nm. However, in our experiment, the tunneling current is still effective where the oxide layer is 7.8 nm. This is probably due to slight doping during the synthesis of the SiC NW, which provides few original defects and decreases the barrier at the heterointerface. If the heterointerface is modified by a fs laser, corresponding to the reduction of the SiO_2 insulator layer, the probability of

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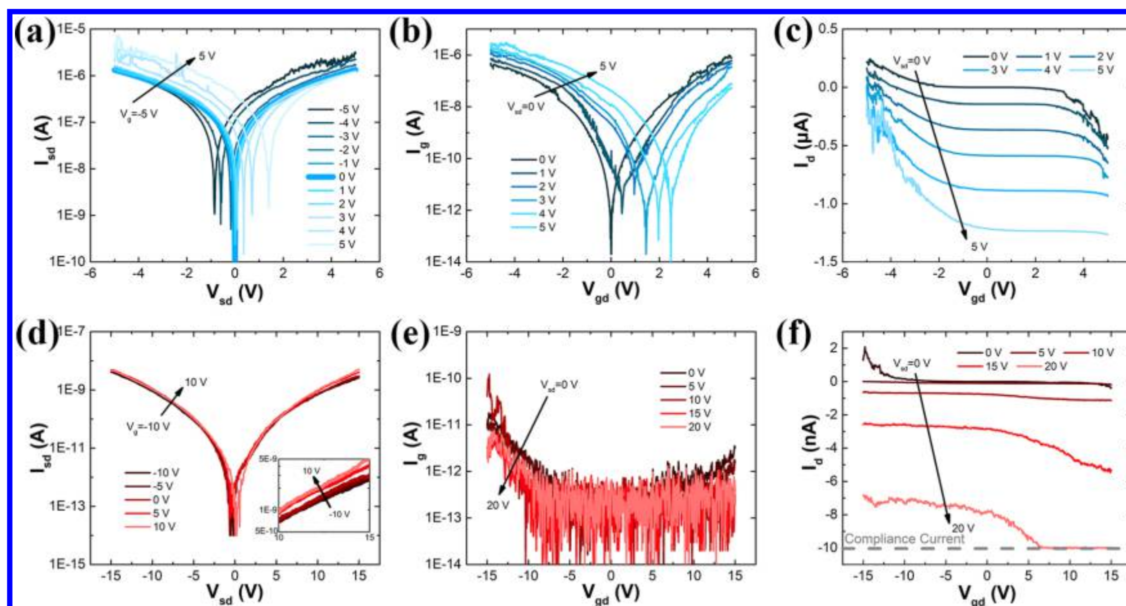

Figure 8. $I-V$ characteristics of three-terminal structures under different gate voltages. The thicknesses of the initial SiO_2 shell are (a)−(c) 7.8 nm and (d)−(f) 35.7 nm, respectively. The output source−drain current in the semi-log scale at gate voltages (a) −5 → 5 V and (d) −10 → 10 V. The output leakage gate current in the semi-log scale at source−drain voltages (b) 0 → 5 V and (e) 0 → 20 V. Output leakage drain current in the linear scale at source−drain voltages (c) 0 → 5 V and (f) 0 → 20 V.

electrons tunneling increases (Figure 7b). Meanwhile, carrier injection into the SiO_2 occurs as the applied voltage continuously increases, resulting in space-charge-limited current.[34] When the injection is weak, the oxide charge density is negligible and the electric field is therefore constant. However, if the SiO_2 layer is reduced drastically, the injection becomes strong, and the current can be expressed as[35,36]

$$I \sim (V - V_0)^m \quad (2)$$

where V_0 is a constant and m is an ideality factor much larger than 2. It is fitted well by the $I-V$ curve of the thinned 7.8 nm SiO_2/SiC NW: the fitted ideality factor is about 5.4 when the bias voltage is >1.8 V (Figure 4a). In this case, a part of the electrons are excited thermally in the SiC, which enables them to come across the barrier from the tunneling process to thermionic emission (exponential fitting in Figure 4a).[37,38]

Taking advantage of the selective thinning by fs laser, a core−shell nanowire-based FET is demonstrated. Figure 8a shows the $I-V$ curves of the SiC NW with an average oxide shell thickness of 7.8 nm. When V_g is 0 V, I_{sd} increases significantly, compared with that in Figure 3d. However, when V_g is applied, the leakage gate current (I_g) can reach ∼1.2 μA at +5 V gate voltage (Figure 8b), due to the decrease of the reverse barrier and the increase of the source−drain current density. Although the gate contact is not modified, the increased carrier density inside the NW will improve the probability of electron tunneling through the Au/SiO_2/SiC heterointerface at the gate. Drain current versus gate voltage characteristics are shown in Figure 8c to highlight the subthreshold characteristics of the device. The largest leakage current at gate contact occurs when the gate-source voltage reaches the maximum value.

To solve the problem of the gate leakage current behavior, fs laser irradiation is utilized to modify the NW−electrode contact with a 35.7 nm SiO_2 shell. To make sure that the SiO_2 layer is thinned enough, the irradiation time is no less than 120 s. In this case, there is no obvious leakage current, and the $I-V$ curves exhibit a typical n-type semiconductor property (Figure 8d). The core/shell structure demonstrates new possibilities to construct single NW-based FET devices, although the I_{sd} drops by several orders of magnitude. The maximum leakage gate current is only ∼10 pA, which can be neglected (Figure 8e). Also, the device shows excellent stability of I_{sd} with the gate voltage ranging from −15 to 15 V (Figure 8f). The SiO_2 layer, directly synthesized on the SiC NW surface, combines well with the core SiC, which is beneficial to the maximum reduction of contact resistance at the SiO_2/SiC interface. Compared with film deposition, selective fs laser irradiation could realize maskless interfacial barrier modification. Meanwhile, combined with an automatically controlled platform, this process has the ability for further modification at the MOS interface in large areas, which shows great potential in complicated nanoelectrical device fabrication.

■ CONCLUSIONS

Plasmonic effect-induced localized interface thinning at the Au/SiO_2/SiC heterointerface has been achieved using fs laser irradiation. A three-terminal structure by constructing core−shell SiC/SiO_2 NWs on Au electrodes is used to test the electron conduction after modifying the interface locally. After fs laser irradiation at a fluence of 72.9 mJ cm^{-2} for 10 s, the current response of the SiC NW with a thin oxide layer (∼7.8 nm) exhibits an obvious conduction improvement with the switching voltage tuning from 15.7 to 1 V, whereas the SiC NW with a thick oxide layer (∼35.7 nm) shows no obvious change under the same condition. The TEM image of the cross section at the modified interface shows that the thickness of the SiO_2 shell can be thinned from 37.8 to 14.2 nm after irradiation for 120 s. Numerical simulations confirm that plasmon-enhanced electric field distribution is confined within the SiO_2 shell, which facilitates intense absorption of the incident laser energy, resulting in the oxide layer thinning and band tuning. Electron tunneling can then be promoted by controlling the thickness of the SiO_2 shell insulator. By

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applying gate voltage on this SiC NW structure, the leakage current can be controlled accordingly, which shows the possibility to precisely adjust the barrier structures even at the nanoscale in electronics.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b20860.

> Geometry models of simulated structures, TEM images and EDX results of core/shell SiC/SiO_2 nanowires, SEM image and electrical properties of pure SiC nanowire, EDX mappings of the heterointerface, and part of the simulation results (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. The authors thank the State Key Laboratory of Tribology in Tsinghua University for making TEM lamella, and Prof. Peng Peng and PhD student Guanlei Zhao for fruitful discussion.

Notes

The authors declare no competing financial interest.

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